WHAT IS CLAIMED IS:

1. An apparatus comprising a symmetric differential domino carry generate circuit having true inputs and compliment inputs, wherein the load for the true inputs is equal to the load for the compliment inputs.

2. The apparatus of claim 1, wherein the circuit also has a true carry generate output and a compliment carry generate output, and wherein the output drive strength for said true output is the same as the output drive strength for said compliment output.

3. The apparatus of claim 1, wherein the circuit further comprises:

a first evaluation block having a plurality of transistors, wherein a number *p* of said transistors are connected in a parallel relationship and a number *s* of said transistors are connected in a serial relationship; and

a second evaluation block having a plurality of transistors, wherein in the second evaluation block *p* transistors connected in a parallel relationship and *s* transistors connected in a serial relationship.

4. An apparatus comprising a differential domino carry generate circuit having a first evaluation block of switches and a second evaluation block of switches, wherein the first evaluation block and second evaluation block each have the same number switches connected in parallel and each have the same number of transistors connected in series.

5. The apparatus of claim 4, wherein the switches in the first evaluation block and second evaluation block are N-channel metal-oxide semiconductor (NMOS) transistors.

6. The apparatus of claim 5, wherein corresponding transistors in the first evaluation block and second evaluation block are the same size.

7. The apparatus of claim 4, wherein the apparatus further comprises cross-coupled P-channel metal-oxide semiconductor (PMOS) keeper transistors.

8. The apparatus of claim 4, wherein the differential domino carry generate circuit is a first stage in a carry look-ahead adder.

9. The apparatus of claim 4, wherein the differential domino carry generate circuit is a group generate gate.

10. An apparatus comprising:

a first output to provide a precharge value during a precharge phase and a true carry generate value during an evaluation phase;

a second output to provide the precharge value during the precharge phase and the compliment of the true carry generate true during the evaluation phase;

a current input;

a first evaluation block connected to the current input and the first output and having a plurality of transistors, wherein a number of said transistors are connected in a parallel relationship and a number of said transistors are connected in a serial relationship; and

a second evaluation block connected to the current input and the second output and having a plurality of transistors, wherein the second evaluation block has the same number of transistors connected in a parallel relationship as the first evaluation block and the same number of transistors connected in a serial relationship as the first evaluation block.

11. The apparatus of claim 10, wherein the output drive strength for the first output is the same as the output drive strength for the second output.

12. The apparatus of claim 10, wherein the current input is a transistor having a source node connected to ground and a gate connected to the clock input.

13. The apparatus of claim 10, wherein circuit further comprises a clock input to receive a clock having precharge and evaluation phases.

14. The apparatus of claim 13, wherein the gate of each transistor in the first evaluation block is connected to one of a set of true inputs and the gate of each of the transistors in the second evaluation block is connected to one of a set of compliment inputs, and wherein the load for the true inputs is the same as the load for the compliment inputs.

15. The apparatus of claim 14, wherein the first evaluation block comprises a first transistor with a drain connected to the second output, a second transistor with a drain connected to the source of the first transistor and a source connected to the current input, a third transistor with a drain connected to the second output, a fourth transistor with a drain connected to the source of the third transistor and a source connected to the current input, and a fifth transistor with a drain connected to the source of the fourth transistor and a source connected to the second output.

16. The apparatus of claim 15, wherein the gates of the first transistor and third transistor are connected to a first of the true inputs, the gates of the second transistor and fifth transistor are connected to a second of the true inputs, and the gate of the fourth transistor is connected to a third of the true inputs.

17. The apparatus of claim 16, wherein the precharge block comprises a first precharge transistor connected to a second current input and a second precharge transistor connected to a third current input, and wherein the first and second precharge transistors each have a gate connected to the clock.

18. The apparatus of claim 17, wherein the apparatus further comprises a keeper connected to each of the first output, second output, first evaluation block, and second evaluation block.

19. The apparatus of claim 18, wherein the transistors in the first evaluation block and second evaluation block are N-channel metal-oxide semiconductor (NMOS) transistors, wherein first and second precharge transistor are P-channel metal-oxide semiconductor (PMOS) transistors, and wherein the keeper comprises two PMOS transistors.

20. An apparatus comprising:

a true sum to provide a precharge signal during the precharge phase and the result of a sum function during the evaluation phase;

a compliment sum output to provide the precharge signal during the precharge phase and the compliment of the true sum output during the evaluation phase;

a first evaluation block connected to a current input, the true sum output, and the compliment sum output, wherein the first evaluation block has a plurality of transistors, and wherein a number of said transistors are connected in parallel and a number of said transistors are connected in serial; and

a second evaluation block connected to the current input and the true sum output and having a plurality of transistors, wherein the second evaluation block has the same number of transistors connected in parallel as the first evaluation block and the same number of transistors connected in serial as the first evaluation block.

21. The apparatus of claim 20, wherein the output drive strength for the true sum output is the same as the output drive strength for the compliment sum output.

22. The apparatus of claim 20, wherein the first evaluation block comprises five transistors, wherein the first transistor has a drain connected to the compliment sum output, the second transistor has a drain connected to the source of the first transistor and a source connected to the drain of the fifth transistor, the third transistor has a drain connected to the true sum output, the fourth transistor has a drain connected to the source of the third transistor and a source connected to the drain of the fifth transistor, and the fifth transistor has a source connected to the current input.

23. The apparatus of claim 22, wherein the gate of the first transistor is connected to an exclusive-OR input, the gate of the second transistor is connected to a first generate input, the gate of the third transistor is connected to a compliment exclusive-OR input, the gate of the fourth transistor is connected to a second generate input, and the gate of the fifth transistor is connected to a propagate input.

24. The apparatus of claim 20, wherein the transistors in the first evaluation block and second evaluation block are N-channel metal-oxide semiconductor (NMOS) transistors.

25. A method comprising:

receiving at a first evaluation block three true input values;

receiving at a second evaluation block three compliment input values, wherein the compliment input values are the compliment of the true input values;

processing the true input values at the second evaluation block to provide a carry generate value at a first output by selecting one of a plurality of stacks of transistors in the second evaluation block, wherein each of said stacks of transistors connects a current input to a first output; and

processing the compliment input values at the first evaluation block to provide the compliment of the carry generate value at a second output by selecting one of a plurality of stacks of transistors in the first evaluation block, wherein each of said stacks of transistors connects said current input to a second output, and wherein the first evaluation block and second evaluation block have the same number of stacks of transistors.

26. The method of claim 25, wherein the first evaluation block and second evaluation block have corresponding stacks that have the same number of transistors.

27. The method of claim 25, wherein the method further comprises:

receiving a clock having a precharge phase and an evaluation phase;

providing precharge values at the first output and at the second output during said precharge phase; and

providing the carry generate value at the first output and the compliment carry generate value at the second output during the evaluation phase.

28. The method of claim 27, wherein the method further comprises preventing current from passing through the current input during the precharge phase and enabling current to pass through the current input during the evaluation phase.

29. The method of claim 28, wherein the method further comprises:

providing the output from the first evaluation block to a keeper;

providing the output from the second evaluation block to a keeper; and

providing the carry generate true output and carry generate compliment output during the evaluation phase based upon output from the first evaluation block, second evaluation block, and the keeper.

30. The method of claim 25, wherein the inputs received and outputs provided are symmetrical.